Course Specification

(Postgraduate Programs)

Course Title: Reconfigurable Hardware Accelerators
Course Code: CE6032
Program: Master of Science in Computer Engineering
Department: Computer and Network Engineering
College: College of Computing
Institution: Umm Al-Qura University
Version: 1.0
Last Revision Date: 12/4/2025

Table of Contents

A. General information about the course:

1. Course Identification:

1. Credit hours: (3)					
2. Course type					
A.	☐University	☐College	☒ Department	☐ Track	
B.	☐ Required		☒ Elective		
3. Level/year at which this course is offered: (Level 3 or Level 4)					
4. Course General Description:					
This course on Reconfigurable Computing provides a comprehensive study of the field Reconfigurable Computing. It provides an entry point to the novice willing to move in the research field reconfigurable computing, FPGA and system on programmable chip design. It provides a strong theoretical and practical background to the field of reconfigurable computing, from the early Estrin's machine to the very modern architecture like coarse-grained reconfigurable device and the embedded logic devices.					
5. Pre-requirements for this course (if any)**:**					
1. Fundamnetals of Digital Design 2. Fundamentals of VLSI Design					
6. Co-requirements for this course (if any)**:**					
None					
7. Course Main Objective(s):					
The objective is to provide an in-depth knowledge on Architectures of reconfigurable systems including design and implementation. The concepts of high level synthesis and development on modern FPGA devices are the other key objectives.					

2. Teaching Mode: (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	45	100

3. Contact Hours: (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
	Total	45

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods:

Code	Course Learning Outcomes	Code of PLOs	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Identify challenges in the design of reconfigurable systems and hardware accelerators	K1	Lectures, and reading assignments	Written exams, assignments, projects and oral presentations
1.2	Explain fundamentals of reconfigurable systems and hardware accelerators deign concepts, terminologies and characteristics	K2		
2.0	**Skills**			
2.1	Design and implement modern reconfigurable systems and hardware accelerators	S1	Lectures, project, discussions, tutorials	Written exams, assignments, projects and oral presentations
2.2	Apply principles of reconfigurable systems and hardware accelerators to solve complex problems	S2		
2.3	Communicate effectively through a written report embodying the design, implementation, evaluation of reconfigurable systems and hardware accelerators	S3		
2.4	Evaluate the performance of reconfigurable systems and hardware accelerators	S4		

Code	Course Learning Outcomes	Code of PLOs	Teaching Strategies	Assessment Methods
3.0	**Values, autonomy, and responsibility**			
3.1	Demonstrate commitment to ethical and professional responsibilities in reconfigurable systems and hardware accelerators	V1	Lectures, project, discussions, assignments and projects	Group assignments and projects
3.2	Work in a team to implement a project in reconfigurable systems and hardware accelerators	V2	Group assignments and projects	Group assignments and projects

C. Course Content:

No	List of Topics	Contact Hours
1.	**Architecture of Reconfigurable Systems:** Exhaustive description of existing reconfigurable architectures, from the simple PLDs to very complex FPGAs and coarse-grained technologies	6
2.	**Low-level Synthesis of reconfigurable devices (RD):** State of the art algorithms for FPGA synthesis, in particular for the Look-up table technology mapping	6
3.	**High-level synthesis (HLS):** Detailed presentation of high-level synthesis approaches for reconfigurable device. Description of the fundamental difference between HLS for reconfiguration and the general HLS	6
4.	**Temporal Placement:** Algorithms for off-line and for on-line temporal placement with various goals like the efficient computation, efficient resource usage and so on	3
5.	**On-line Communication:** State of the art approaches for realizing dynamic communication paths between components dynamic placed on the chip at run-time	5
6.	**Partial reconfiguration design:** various approaches for designing partial reconfigurable systems on Xilinx FPGAs: tutorial–like presentation of the approaches	5
7.	**Applications:** Applications that may benefit from the use of reconfigurable device are pointed out and the use of reconfiguration to improve the systems is presented	5
8.	Emerging Trends in Reconfigurable Hardware Accelerators	9
	Total	45

D. Students Assessment Activities:

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Assignment	3, 6, 9 and 12	30
2.	Projects	13	40
3.	Presentation of scientific article		30

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.)

E. Learning Resources and Facilities:

1. References and Learning Resources:

Essential References	Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications by Christophe Bobda, Springer Science, 2007, ISBN: 978-9048175314
Supportive References	The FPGA Programming Handbook: An essential guide to FPGA design for transforming ideas into hardware using SystemVerilog and VHDL, 2nd ed. Frank Bruno, and Guy Eschemann, Packt Publishing Ltd, 2024, ISBN-10 : 1805125591, ISBN-13 : 978-1805125594 Robotic Computing on FPGAs (Synthesis Lectures on Computer Architecture) by Shaoshan Liu, Zishen Wan, Bo Yu, and Yu Wang, Springer, 2021, ISBN-10 : 3031006437, ISBN-13: 978-3031006432 Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation, Scott Hauck and André DeHon, Morgan Kaufmann, 2007, ISBN: 978-0123705228 (print), 978-0080556017 (eBook)
Electronic Materials	The instructor may provide as per requirements
Other Learning Materials	The instructor may provide as per requirements

2. Educational and Research Facilities and Equipment Required:

Items	Resources
Facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Classrooms
Technology equipment (Projector, smart board, software)	Projector
Other equipment (Depending on the nature of the specialty)	

F. Assessment of Course Quality:

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	Students, Program Leaders	Indirect
Effectiveness of students' assessment	Program Leaders	Direct
Quality of learning resources	Students, Faculty	Indirect
The extent to which CLOs have been achieved	Students, Faculty, Program Leaders	Direct and Indirect
Other		

Assessor (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval Data:

COUNCIL /COMMITTEE	**Computer and Network Engineering Department Council**
REFERENCE NO.	**The 18th Session Of The Academic Year 1446**
DATE	**15/4/2025**