

Ch1: Digital Systems and Binary Numbers
Ch2: Boolean Algebra and Logic Gates
Ch3: Gate-Level Minimization
Ch4: Combinational Logic
Ch5: Synchronous Sequential Logic
Ch6: Registers and Counters

Chapter 6

Registers and Counters

Switching Theory & Logic Design
1403271-4

Prof. Adnan Gutub

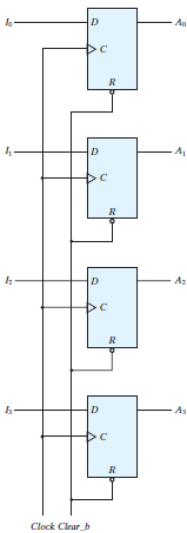
Main Ref: M. Morris Mano and Michael D. Ciletti, Digital Design, Prentice Hall

Content

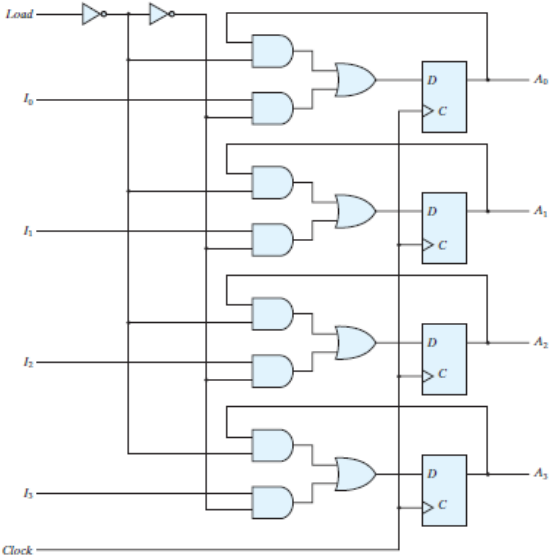
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6.1 Registers
4-bit Register



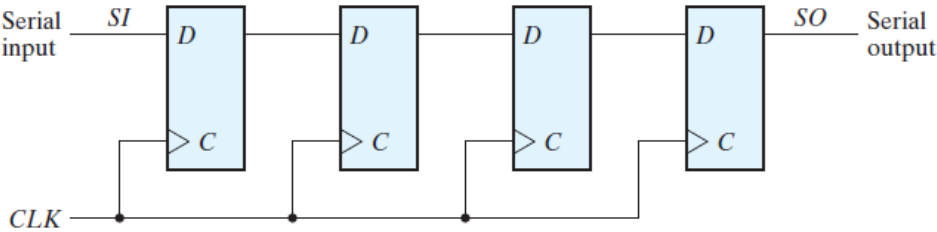
Register with Parallel Load



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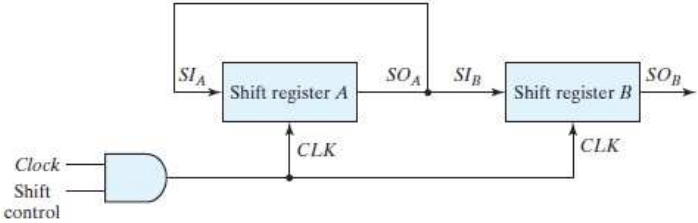
6.2 Shift Registers

4-bit shift register

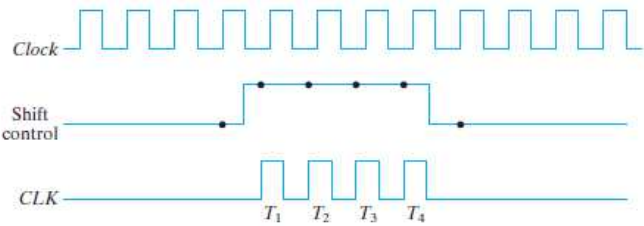


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Serial Transfer Shift Register



(a) Block diagram

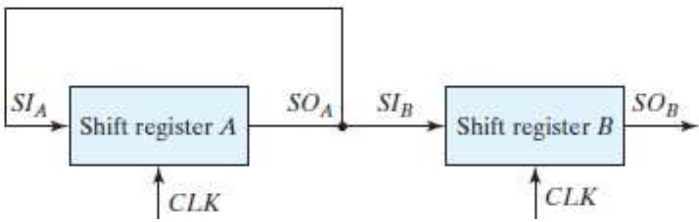


(b) Timing diagram

FIGURE 6.4
Serial transfer from register A to register B

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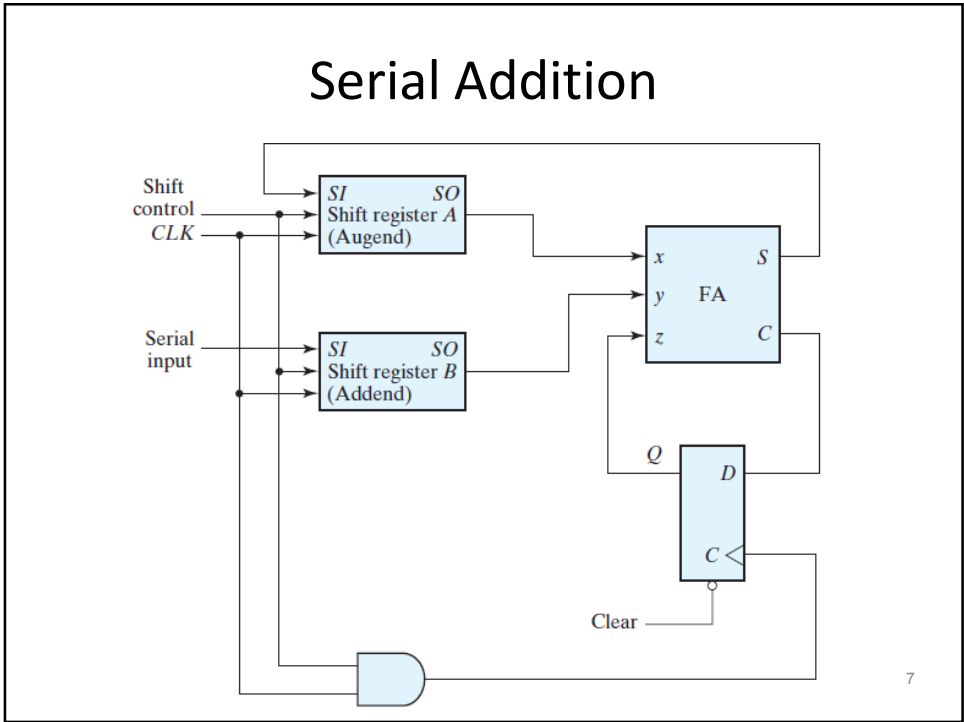
Serial Transfer Shift Register Example



Serial-Transfer Example

Timing Pulse	Shift Register A				Shift Register B			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

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State Table for Serial Adder to use JK FF

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J _Q	K _Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

$$J_Q = xy$$
$$K_Q = x'y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$

The diagram illustrates a serial adder circuit. It features two shift registers, A and B, and a J-K flip-flop. The shift registers are clocked by a common CLK signal. The serial input is connected to the SI input of both shift registers. The SO output of shift register A is labeled x, and the SO output of shift register B is labeled y. The outputs x and y are connected to the inputs of an AND gate and an OR gate. The output of the AND gate is connected to the J input of the J-K flip-flop. The output of the OR gate is connected to the K input of the J-K flip-flop. The J-K flip-flop is also clocked by the CLK signal. The output of the J-K flip-flop is connected to the S input of an OR gate. The output of the OR gate is labeled S. The circuit also includes a Clear input for the J-K flip-flop.

Shift control

CLK

Serial input

SI

SO

Shift register A

x

SI

SO

Shift register B

y

J

C

K

S

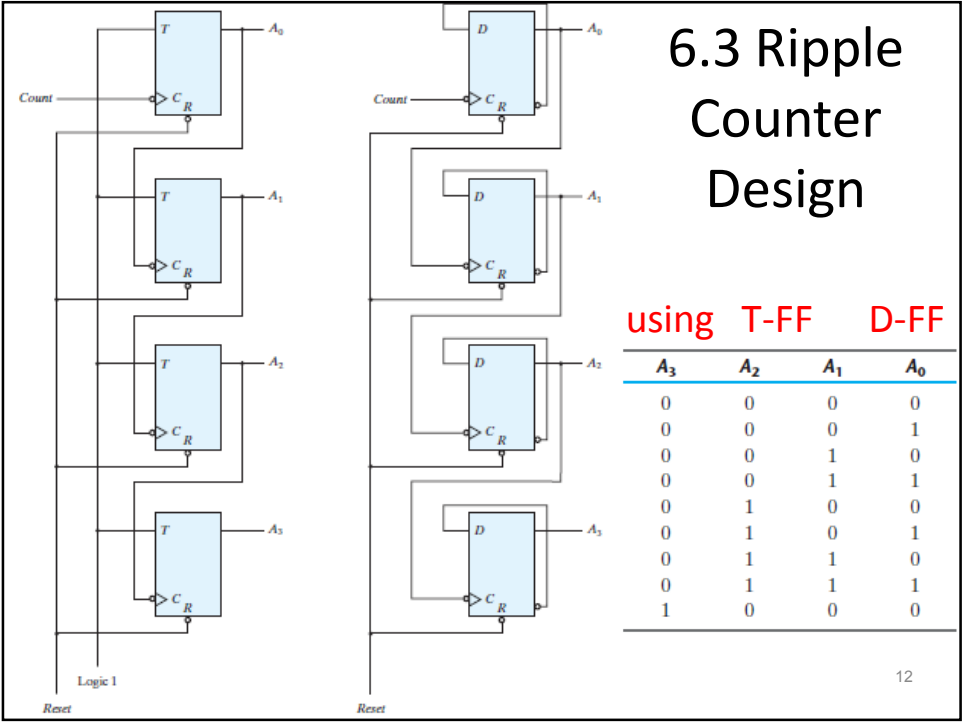
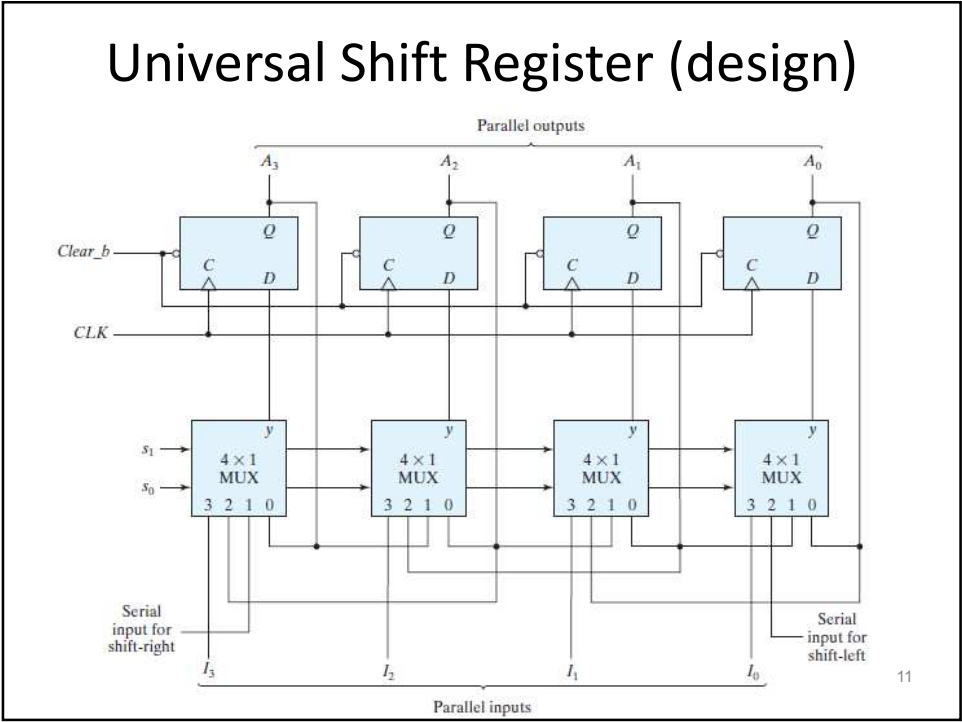
Clear

$J_Q = xy$

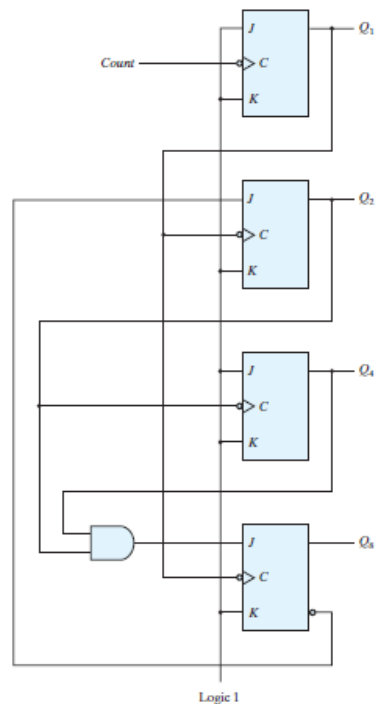
$K_Q = x'y' = (x + y)'$

$S = x \oplus y \oplus Q$

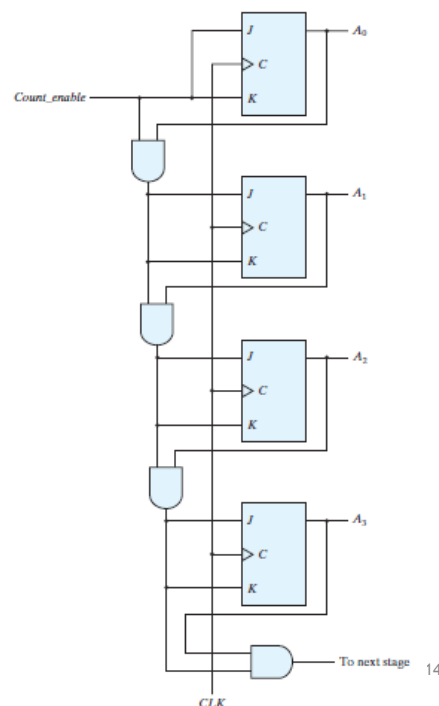
Mode Control		Register Operation
s_1	s_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load



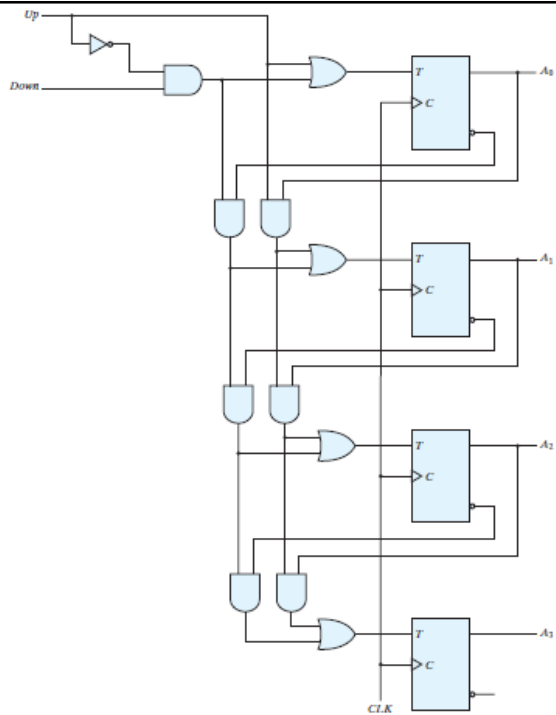
state diagram



Synchronous
Counters have
independent signal
CLK affecting FFs
Counting



Up-Down
Binary
Counter



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BCD Counter

State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q ₈	Q ₄	Q ₂	Q ₁	Q ₈	Q ₄	Q ₂	Q ₁	y	TQ ₈	TQ ₄	TQ ₂	TQ ₁
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

$T_{Q1} = 1$
 $T_{Q2} = Q_8'Q_1$
 $T_{Q4} = Q_2Q_1$
 $T_{Q8} = Q_8Q_1 + Q_4Q_2Q_1$
 $y = Q_8Q_1$

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