Chapter 6
Registers and Counters

Switching Theory & Logic Design
1403271-4

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Main Ref: M. Morris Mano and Michael D. Ciletti, Digital Design, Prentice Hall

Content

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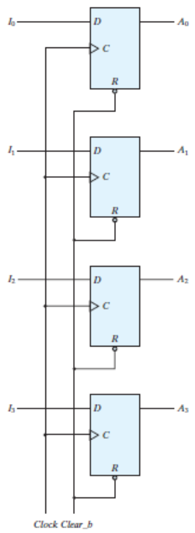
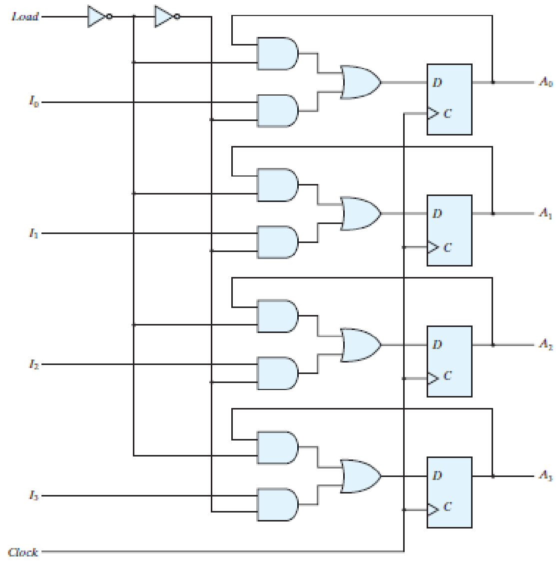
6.1 Registers

4-bit Register



Register with Parallel Load



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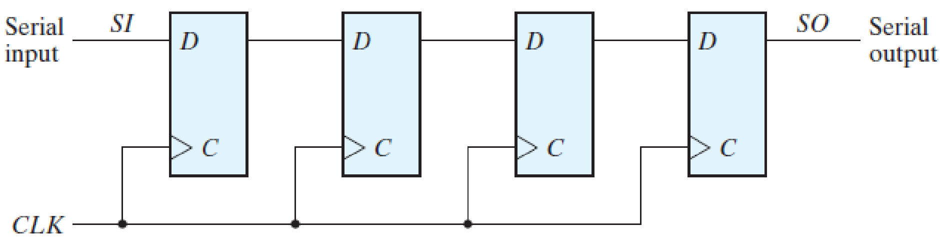
6.2 Shift Registers

4-bit shift register



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Serial Transfer Shift Register

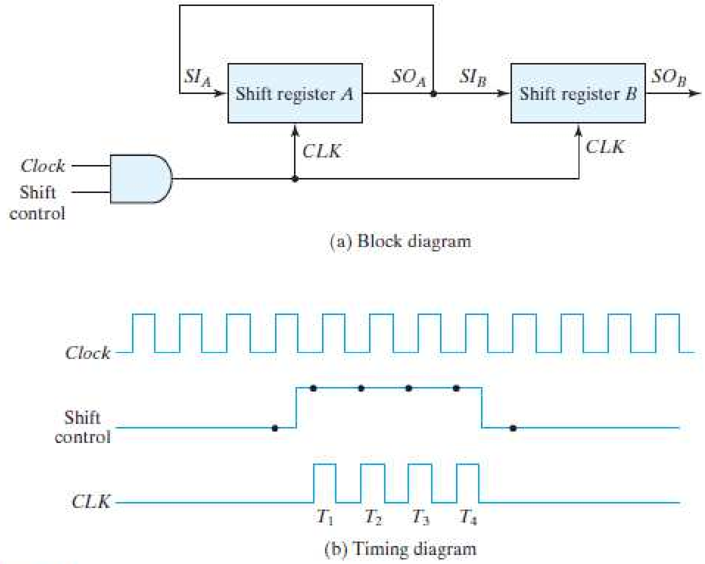

FIGURE 6.4
Serial transfer from register *A* to register *B*

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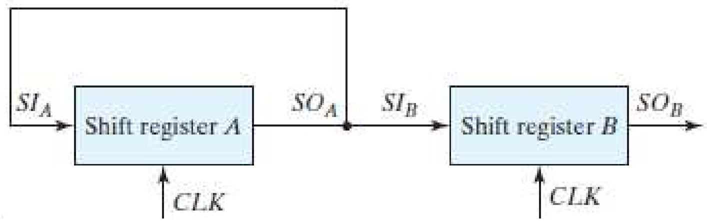
Serial Transfer Shift Register Example



Serial-Transfer Example

Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

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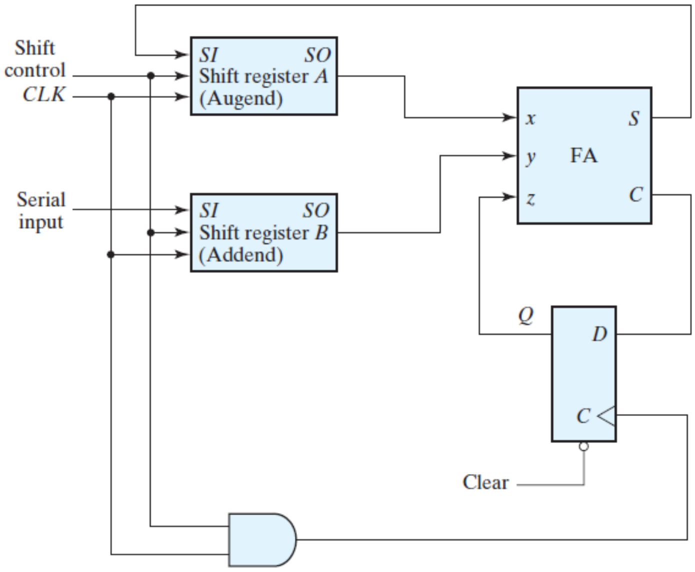
Serial Addition



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State Table for Serial Adder

to use JK FF

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

$$J_Q = xy$$
$$K_Q = x'y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$

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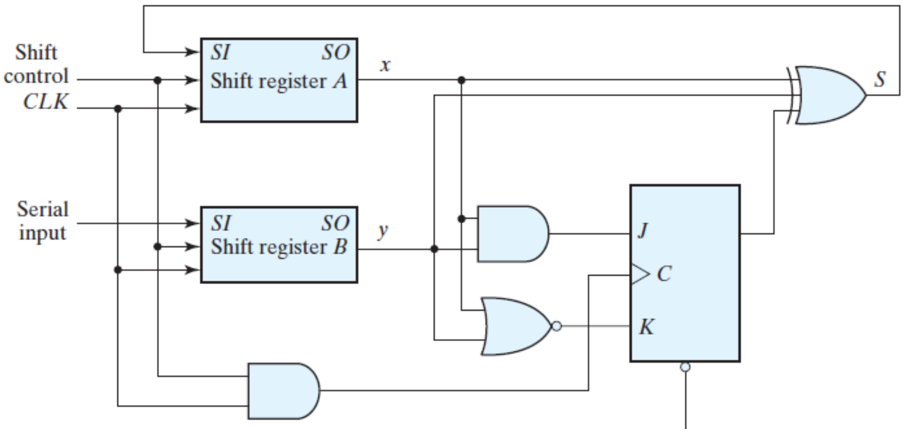
Second form of serial adder
to use JK FF



$J_Q = xy$

$K_Q = x'y' = (x + y)'$

$S = x \oplus y \oplus Q$

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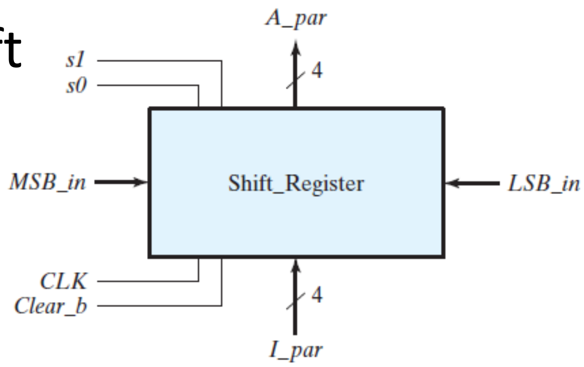
Universal Shift Register (idea)



Function Table for the Register of Fig. 6.7

Mode Control		
s_1	s_0	**Register Operation**
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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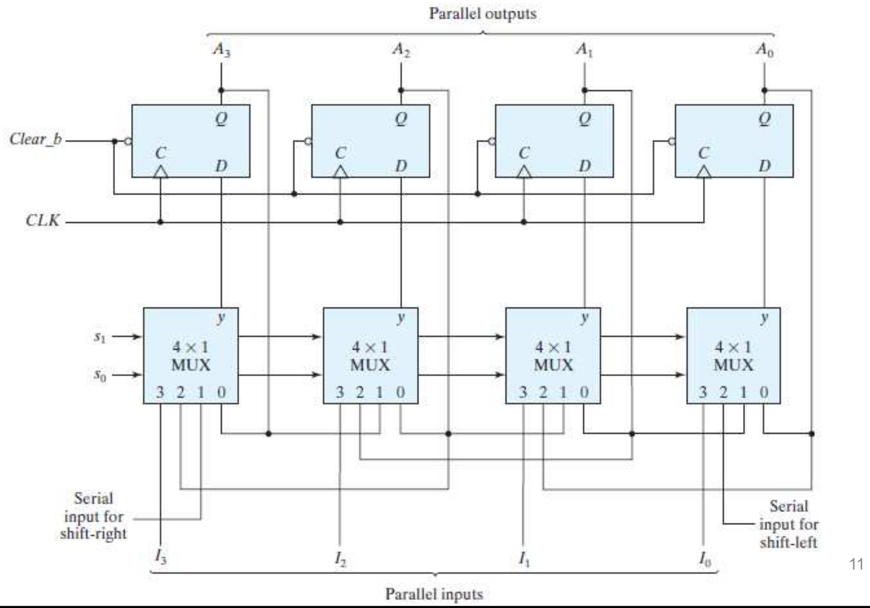
Universal Shift Register (design)



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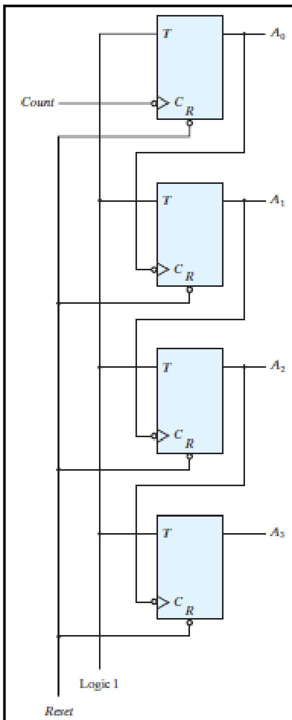

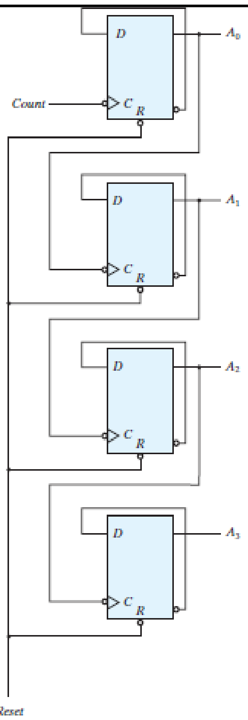

6.3 Ripple Counter Design

using T-FF D-FF

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

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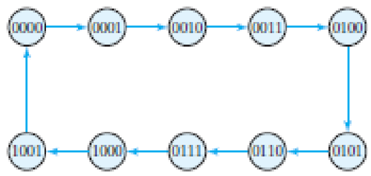
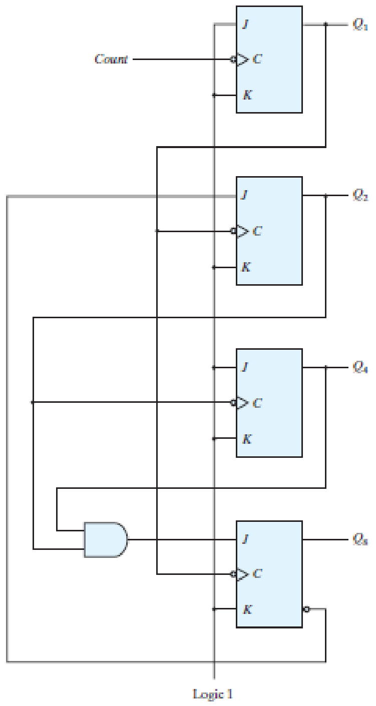
BCD Ripple Counter Design



state diagram



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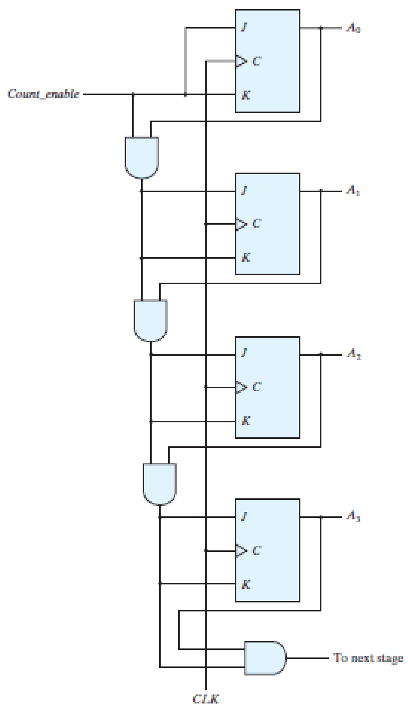
6.4 Synchronous Counters

Binary Counter

Synchronous Counters have independent signal CLK affecting FFs Counting



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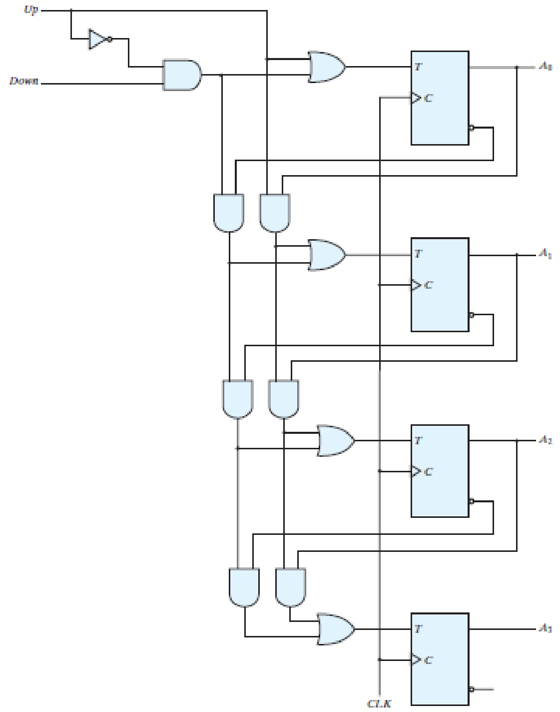
Up–Down Binary Counter



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BCD Counter

State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

$$T_{Q1} = 1$$
$$T_{Q2} = Q'_8Q_1$$
$$T_{Q4} = Q_2Q_1$$
$$T_{Q8} = Q_8Q_1 + Q_4Q_2Q_1$$
$$y = Q_8Q_1$$

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